REMARKS/ARGUMENTS

Applicants have received the Office action dated June 13, 2005, in which the Examiner: 1) rejected claims 25-26 and 29-30 as obvious over Watanabe (U.S. Patent No. 6,259,753); 2) allowed claims 1-24 and 33-44; and 3) concluded that dependent claims 27, 28, 31, and 32 contain allowable subject matter. Applicants traverse the claim rejections for the following reasons.

The Examiner focused the rejections of claims 25-26 and 29-30 on Figure 5 of Watanabe. As described in columns 9 and 10 of Watanabe, Figure 5 shows four pattern matching circuits 541-544. Each matching circuit compares a certain four bits from an input bit stream to a four-bit predetermined sync pattern. The sync pattern is different for each matching circuit. The function of the logic in Figure 5 is to determine whether the 16-bit input bit stream matches a specified 16 bit synch pattern. The logic of Figure 5 makes the determination by examining in parallel four-bit sub-portions of the input bit stream. The output signal from each matching circuit (signals 545-548) is a single bit that specifies whether that particular matching circuit determined that its four-bit input correctly matched the four-bit predetermined sync pattern corresponding to that matching circuit. A logic "1" indicates that there was a match and a logic "0" indicates there was no match. The adder/majority decision circuit 551 receives the four matching result signals 545-548, adds the signals together, compares the sum to a threshold, and outputs a synch signal detection output signal if the sum at least equals the threshold value.

Claim 25 is directed to a "method of locating and indicating the position of a leading binary bit value in an input string of bits." Watanabe does not disclose such a method. Watanabe simply looks for a sync bit pattern in a bit stream, but does not locate and indicate the position of a leading binary bit value in an input bit string. Claim 25 specifically requires "locating the position of the leading binary bit value in each substring and generating a first binary representation of this position for each substring." Watanabe does not do this. Instead, Watanabe determines if each four-bit sub-portion matches a four-bit sync pattern.

Watanabe also does not disclose "combining the first binary representation corresponding to the most significant substring and the second binary representation to form a single output binary representation of the position of a leading binary bit value in the input string." The Examiner contends otherwise alleging that the decision circuit 551 "combines the matching results to form a sync pattern representative of binary representation of the position of leading binary bit value of the input string." Office action page 3. As explained above, however, the decision circuit 551 adds the matching signals together, compares the sum to a threshold, and outputs a synch signal detection output signal if the sum at least equals the threshold value. The matching signals are combined together in Watanabe, but are not combined together "to form a single output binary representation of the position of a leading binary bit value in the input string."

Claim 25 also requires "identifying a most significant substring that includes the most significant bit value in the input string and generating a second binary representation of this substring." The Examiner acknowledged that Watanabe fails to disclose this limitation, but for some reason the Examiner does not seem troubled by this deficiency of Watanabe. At any rate, Watanabe naturally does not disclose this act of identifying as claimed, as well as the other limitations noted above, because the purpose of Watanabe's logic is not to locate and indicate the position of a leading bit value in a bit string as explained above.

For any or all of the reasons noted above, claim 25 is not anticipated by nor rendered obvious in light of Watanabe. Claim 26, which depends from claim 25, is also allowable for the same reasons as claim 25.

Although referring to a "trailing" binary bit value and not a "leading" binary bit value as in claim 25, claim 29 is patentable for some, if not all, of the reasons explained above with regard to claim 25. Claim 30 depends from claim 29 and thus is allowable for the same reasons as claim 29.

Applicants respectfully request reconsideration and that a timely Notice of Allowance be issued in this case. It is believed that no extensions of time or fees are required, beyond those that may otherwise be provided for in documents

accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required (including fees for net addition of claims) are hereby authorized to be charged to Hewlett-Packard Development Company's Deposit Account No. 08-2025.

Respectfully submitted,

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